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6

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1. PURPOSE

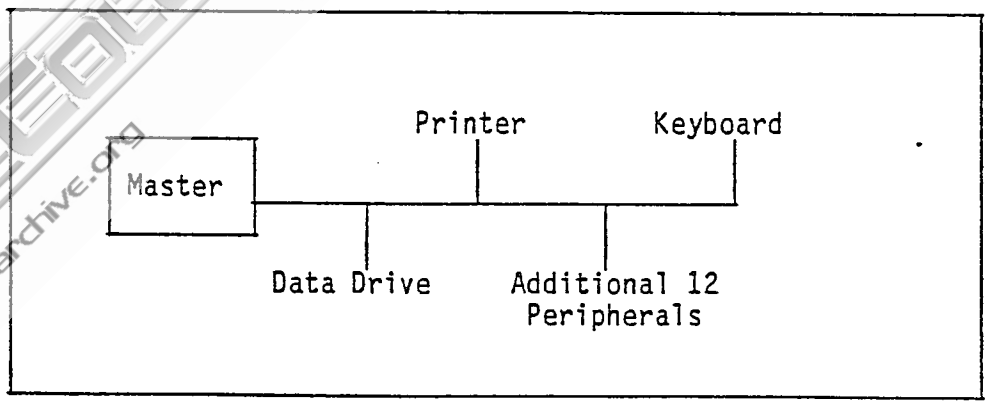
This specification establishes the engineering specification and criteria for the performance of the AdamNet Communication Network for the Adam home computer system.

2.0 GENERAL DESCRIPTION

AdamNet is the serial communications link which provides an asyncronous means of communication to the Adam home computer system. The network is designed to be controlled by a 6801 master which has the capability to communicate with up to 15 peripheral devices (referred to as slaves) including other Adam computer systems.

The functional design of the network is shown in Figure 1. The horizontal line is a network that connects the peripheral devices to the master, which physically resides inside the Delta or Gamma CPU. The network is controlled by the master which sends tokens, via the network, to all peripheral devices, and individually peripheral devices return tokens, via the network, to the master.

Figure 1



The network is represented with three wires: data (transmit/receive), reset and signal ground. The data line is a half-duplex, serial line on which all communication between master and peripherals is performed. The reset line behaves as a master reset signal to each and every node attached to the network. Communication on this line is one way, meaning there is no provision for a response by any node. When reset has been activated, all nodes are sent a signal and then brought to initialization. The signal ground wire which is required to complete the current path without introducing noise, is used as a reference level for the reset and transmit/receive line.

3.0 TECHNICAL DESCRIPTION

3.1 Baud Rate

The baud rate is 62,500 bps and is derived by using the external 4.0 MHz crystal and the internal divide by 16 option. The time to transmit one byte, including start and end bit is 160 microseconds.

3.2 Data Format

The data format is NRZ (non return to zero) with 8 data bits, a start bit which is defined as being the mark level and a stop bit which is defined as being the idle level.

3.3 Communications Protocol

The communication protocol is a half duplex bidirectional serial line.

3.4 Network Protocol

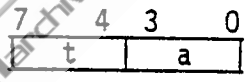
The network protocol is based on passing information via tokens. Tokens passed from the master to the slaves are called command tokens, and tokens passed from the slaves to the master are called response tokens. Tokens may be either a one byte control message or a multiple byte data message.

TOKEN TABLE

TYPE.SUBTYPE	MESSAGE	Token Code	Token Length Byte(s)
COMMAND.CONTROL	RESET	0	1
	STATUS	1	1
	ACK	2	1
	CLR	3	1
	RECEIVE	4	1
	CANCEL	5	1
	NACK	7	1
	READY	13	1
COMMAND.DATA	SEND	6	4+data
RESPONSE.CONTROL	STATUS	8	4
	ACK	9	1
	CANCEL	10	1
	NACK	12	1
RESPONSE.DATA	SEND	11	4+data

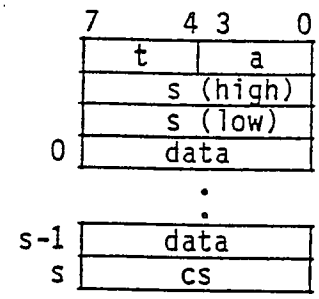
Tokens formats are as follows:

1 BYTE CONTROL TOKEN:



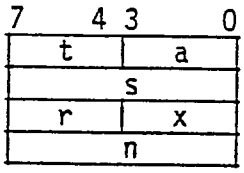
	COMMAND.CONTROL	RESPONSE.CONTROL
t:	token code	token code
a:	target address: 1-15,	source address: 1-15

MULTIPLE BYTE DATA TOKEN:



	COMMAND.DATA	RESPONSE.DATA
a:	target address: 1-15	source address: 1-15
t:	send 6 (token code)	send: 11 (token code)
s:	no. of data bytes 0 - 64K	no. of data bytes 0 - 64K
data:	data byte	data byte
cs:	checksum	checksum

SPECIAL RESPONSE.CONTROL (STATUS):



a: source address: 1-15
t: status: 8 (token code)
s: max message size: 0-64K
x: transmit code 0= character mode: 0-127
1= byte mode: 0-255
2= vector mode: array of bytes
3= block mode
r: reserved
n: node type (0-255)

4.0 Functional Description

4.1 Initialization

Upon power up, the Z80 performs a hard reset of the network via the reset line and sets the Process Control Block (PCB) to a default address of FECO H. The PCB is the area in memory used by the Z80 and and master 6801 to communicate. The Z80 and the master 6801 then syncronize themselves by writing to a common memory location. Next, the Device Control Blocks (DCB) and PCB memory are zeroed out. Status requests are then sent to each possible device and a timer started. These requests are individually and sequentially sent to each DCB memory location, starting with the first. If there is a response, then DCB memory is allocated for that device. If within 500 microseconds there is no response, a timeout

will occur. Upon timeout, the Z80 increments the DCB count and returns control to the master 6801. Following a timeout or response, the 6801 sends a status request to the next DCB location until all DCB locations receive a request.

4.2 Normal Operation

The master 6801 looks for commands which the Z80 stores in the 0th byte of every allocated DCB memory location. A DMA mechanism allows the master to continuously scan the DCB's. When a command, anything other than a zero, is read the master 6801 responds. Upon completion of the command, the master stores a one in bit 1 of byte 0 telling the Z80 the command is completed and scans the 0th byte of the next DCB memory location. When a zero is read, indicating no command, the master goes to the next 0th byte.

At this time there is no set node priority although the system is designed so that software can be written to install one at a future date. Presently, the 6801 reads the 0th byte of every DCB memory location in succession, responding to any command and upon completion, it looks for the next command.